Abstracts

Power Design for Gigabit Josephson Logic Systems

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An ac power system design in described for powering, at near gigahertz frequencies, 16K Josephson latching logic circuits distributed uniformly over 16 chips. The power system distributes a sinusoidal current waveform from a single source to the many chip quadrants through a tree system of thin-film transformers that have branching secondaries and multiple turn primaries to maintain nearly constant current amplitudes throughout the system and small phase skews at the logic-circuit level. The sinusoidal waveform is clipped on-chip to provide the trapezoidal waveform required by the logic circuits. The ratio of the duration of the up-portion of the trapezoidal half-cycle to the half-cycle period (the logic cycle) is defined as the active duty cycle for the logic. The 16K circuit-power design is capable of providing an 80-percent duty cycle at a 1.7-ns logic cycle while keeping current levels in the system below 300 mA. An approximate expression is derived that predicts that for any power-system design of this type the product of the system size, the highest frequency of operation, and the chip-quadrant current level is a constant.

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